FASP_04 ASIC for the Transition Radiation Detector with two-dimensional position information for CBM experiment at FAIR

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Technology: ams 0.35µm CMOS C35B4C3 4M
Die Size: 3.4mm x 4mm
Design Tools: Cadence
Application Area: Detectors used in basic research experiments

Introduction

The Fast Analog Signal Processor (FASP) ASIC was designed for Compressed Baryonic Matter (CBM) at the future acceleration facility FAIR, Darmstadt, Germany. The ASICs will be integrated into the Front-End Electronics (FEE) of the Transition Radiation Detector with two-dimensional position information (TRD-2D).

Description

The FASP_ASIC has 16 self-triggered analogic red-out channels, with mixed-signal type circuits for processing the signals provided by 16 consecutive readout pads of the TRD-2D. The ASIC requires interconnection for a continuous readout of the whole active area of the chamber. The signals produced by a charged particle hit in the chamber are distributed on few consecutive pads and processed together, in a self-triggered mode (the channel with the highest signal enables also the processing of the signal of the neighbours). A mixed-signal circuitry is generated to both inter-channel communication within one ASIC as well as between neighbouring ASICs.

For each processed input signal, two output signals are delivered:

a) a flat top analog (peak-sense) signal with adjustable time interval. Two versions, including an option for flat-top or semi-Gaussian output, were also designed and produced.
b) a logical signal lasting 14 clock periods.

Both types of FASP_ASIC outputs are suitable for driving a wide range of ASIC or commercial analog-to-digital converters.

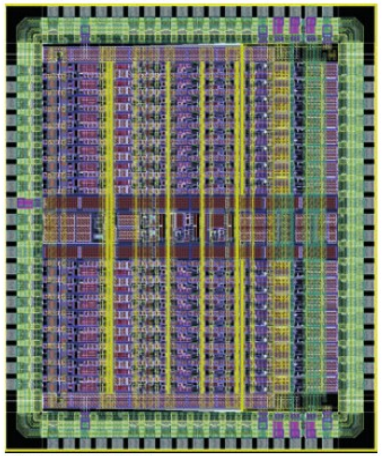

Fig.1: Layout of FASP_04 ASIC.

Fig.2: FASP_04 PCB substrate for flip-chip connection.

Each FASP_ASIC channel contains:

- Charge sensitive preamplifier
- Pole-zero circuit
- Two stages of 2nd order RC filters
- Peak-detector circuit: It detects and maintains the peak value of the RC filters output signal, providing the possibility of two selectable types of the output signal, a semi-Gaussian or/and the peak value (flat-top)

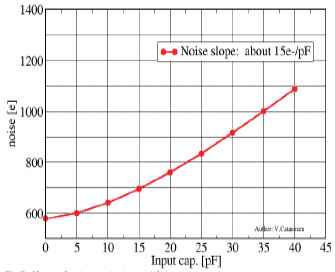

Fig.3: Channel noise variations with input capacitance.

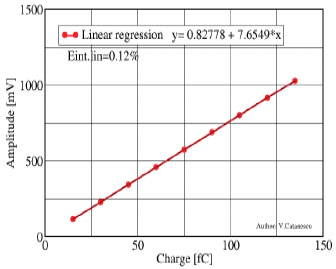

Fig.4: Channel integral nonlinearity.

- Logic circuitry: This part implements self-trigger signals, generating the logic signals for ASIC inter-channel communications and interconnection between the neighbouring ASICs. It also provides the logic signals necessary to connect and synchronize with external ASIC or commercial ADCs

Results

Detailed simulations (i.e. typical, corner, Monte Carlo) were carried out, in schematic and layout. The results of the manufactured chips are presented in the table below.

Detector pad capacitance	25pF
Positive input charge range	0.15fC - 165fC
Input pulse rate	max 2 MHz
Channel gain	6.2 mV/ fC
RC filter shaping time	100 ns
Channel noise ($C_{det.pad}$=25pF)	940 e
Noise variation with det. pad cap.	15e/pF
Channel integral nonlinearity	
semi-Gaussian output	0.12%
peak-sense output	0.06%
Analog output range	0 - 1 V
DC adj. output level	0.2 V - 0.5 V
Peak-sense output plateau width	16 Tck
Semi-Gaussian output FWHM	290 ns
External clock frequency	max 80 MHZ

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Acknowledgements

This work was supported by Romanian Government Ministry of Research Innovation and Digitisation, projects RO-FAIR 03/16.11.2020 and PN 19060103.